iW3658 Application

...personal
...portable
...connected

Agenda

- Key Feature
- Typical Application Schematic
- Basic Application
- Layout Consideration
- Issue sharing
- Calculate sheet introduction
- Summary

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Key Feature

Low cost TRIAC dimmable driver IC

- ✓ Intergrade HV-Mosfet
  - Easy to layout
  - Achieve to design small size SSL driver

- ✓ Single winding Transformer
  - No auxiliary winding for charging Vcc

- ✓ One differential mode inductor for EMI
  - Only π filter for EMI

- ✓ Effective operation mode
  - No dimmer mode and dimmer mode operation distinguished
    - Fixed Vipk control with max Ton limit for Low PF version
    - Constant Ton control for High PF version
  - No bleeder control
    - better for thermal control

Compare with Mini-fire and Street-fire

ITEM \ IC		IW3658	IW3689	IW3688
Package		**SOP - 7**	SOP- 8	SOP - 14
H-V Mosfet		**Intergrade**	Outside	Outside
Input Power		＜13W	**＜25W**	**＜25W**
Thermal		**Low**	High	High
Components	High Line	**20 Pcs**	39	41
	Low Line	**19 Pcs**	34	36
EMI	Inductor	**1 Pcs**	2 Pcs	2 Pcs
	Capacitor	2 Pcs	2 Pcs	2 Pcs
Topology	Buck-boost	√	√	√
	Buck	√	×	×

Key Feature

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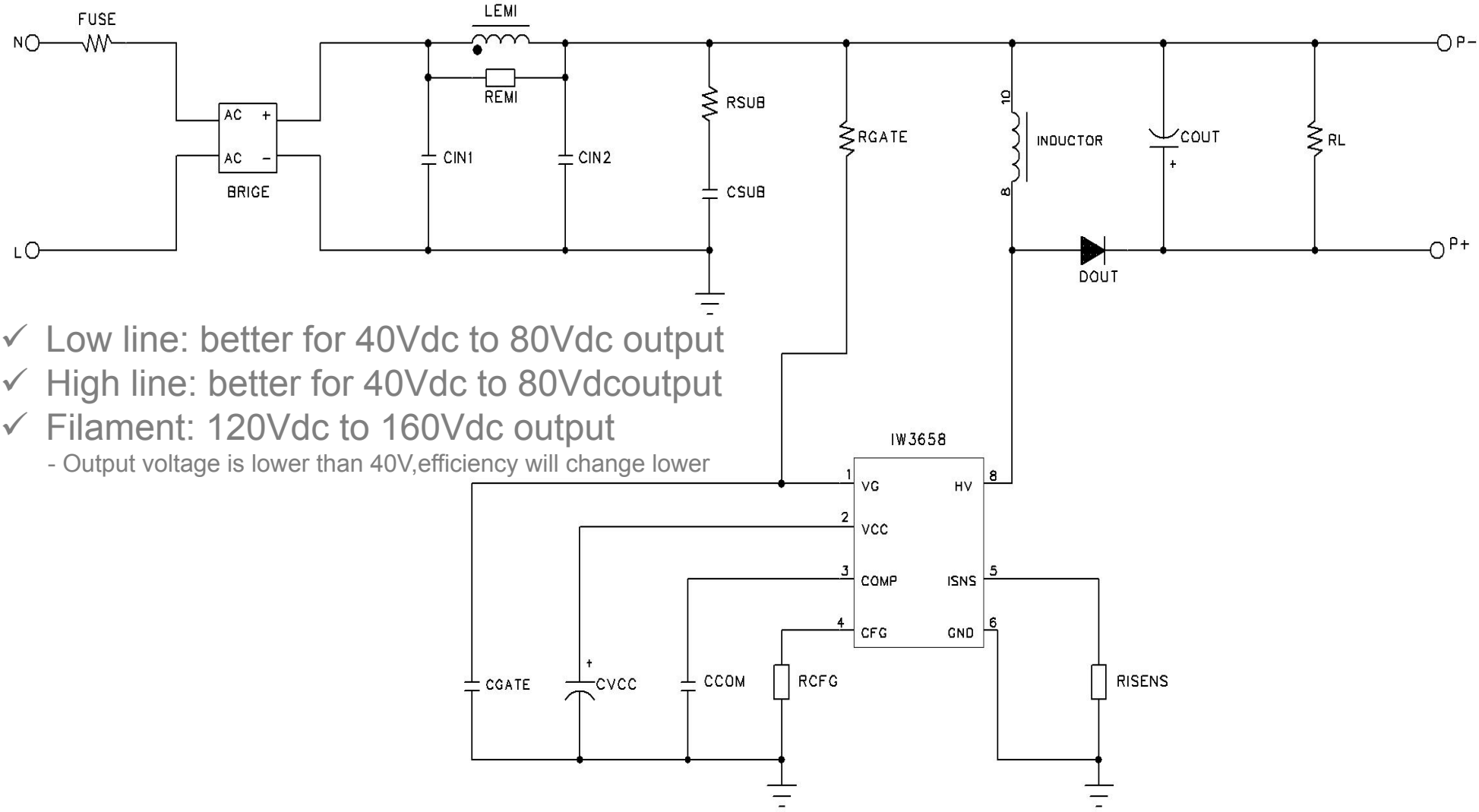
Buck-Boost

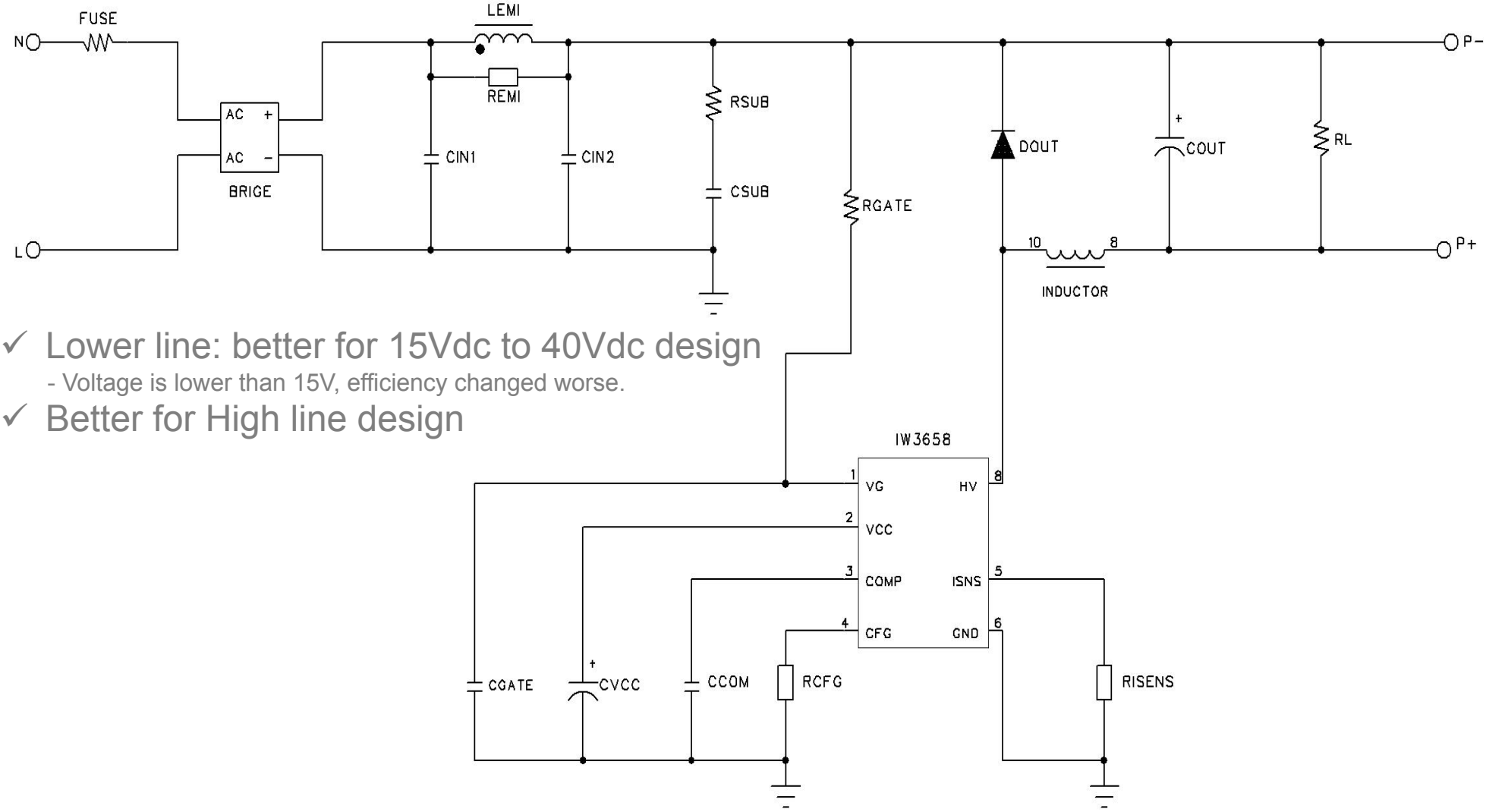
19-20pcs components



- ✓ Low line: better for 40Vdc to 80Vdc output
- ✓ High line: better for 40Vdc to 80Vdcoutput
- ✓ Filament: 120Vdc to 160Vdc output
  - Output voltage is lower than 40V,efficiency will change lower

Buck

19-20pcs components



- ✓ Lower line: better for 15Vdc to 40Vdc design
  - Voltage is lower than 15V, efficiency changed worse.
- ✓ Better for High line design

Key Feature

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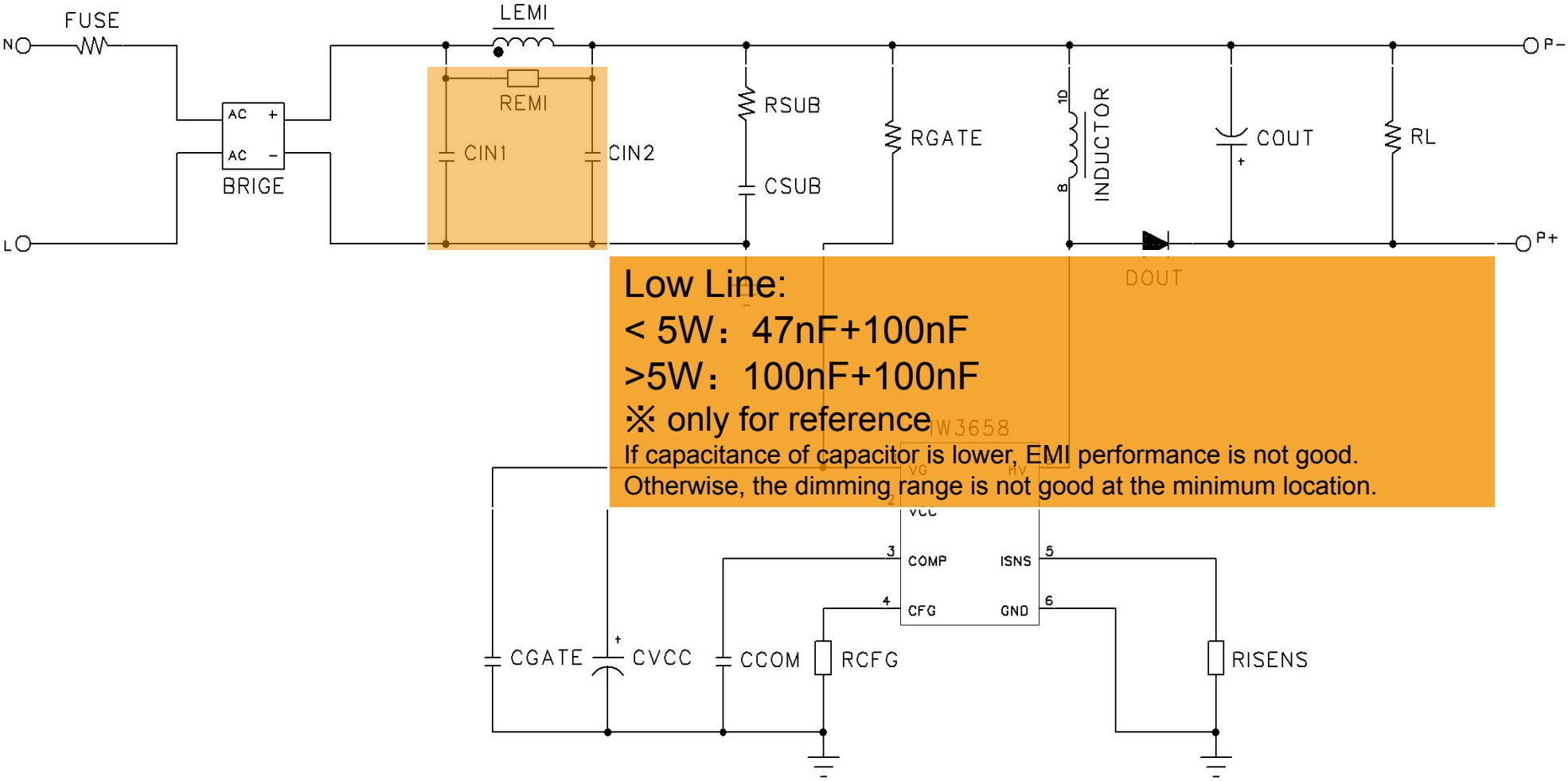
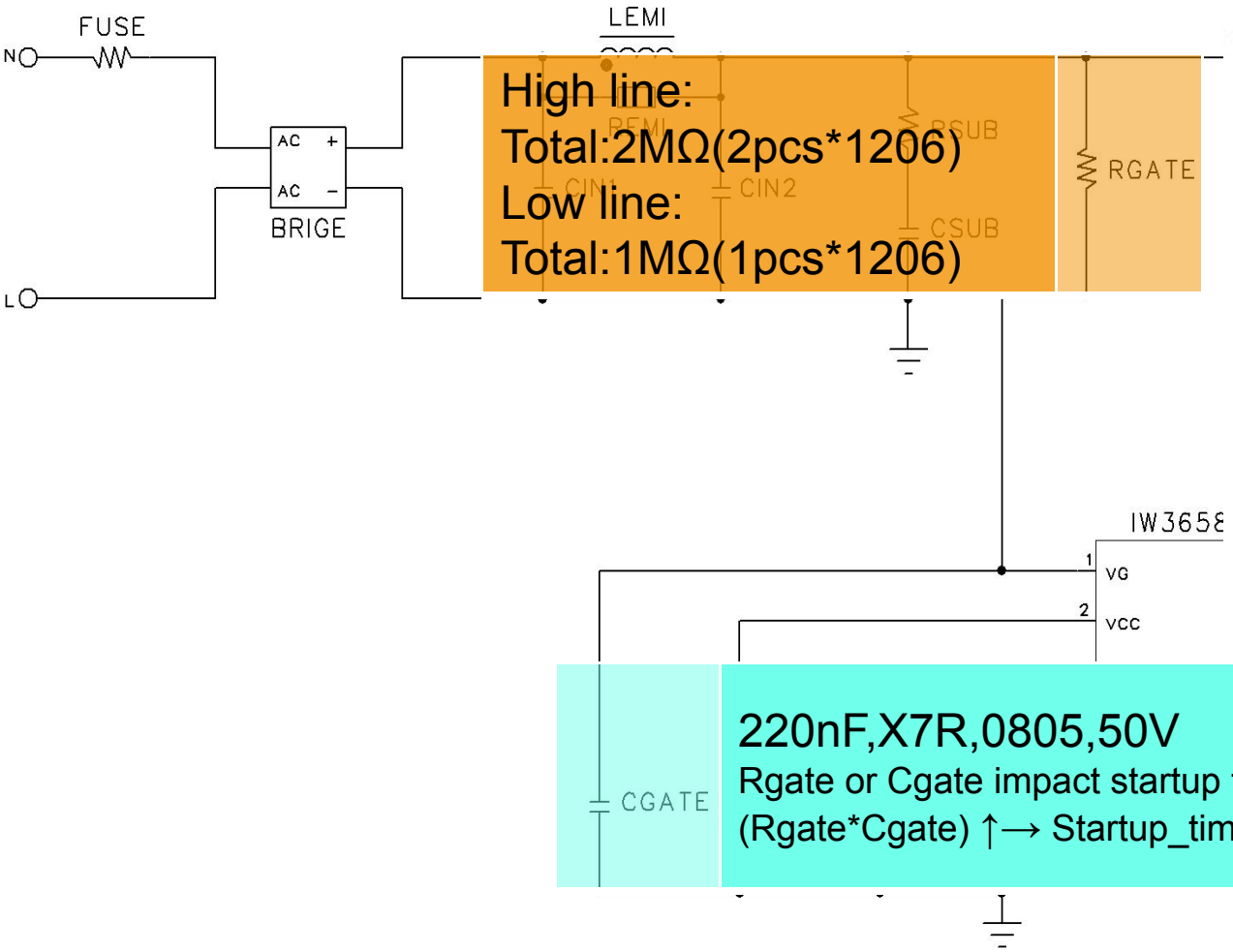
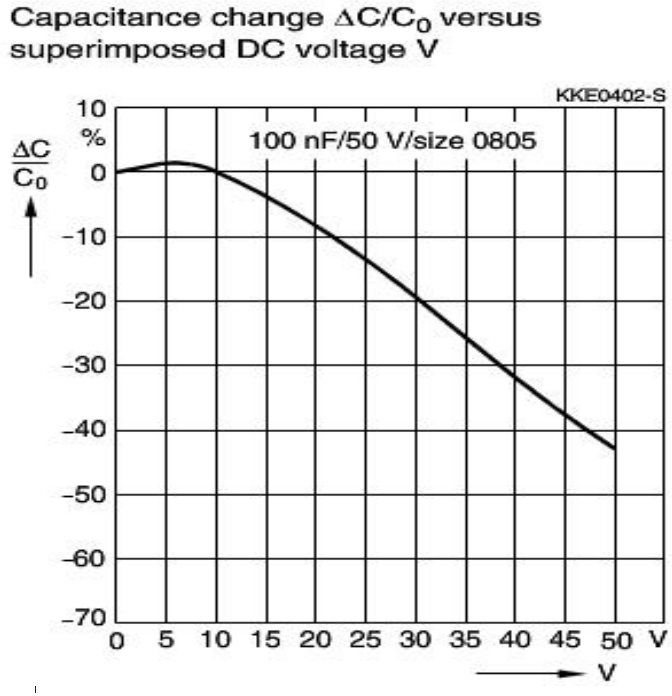
Cin Recommendation

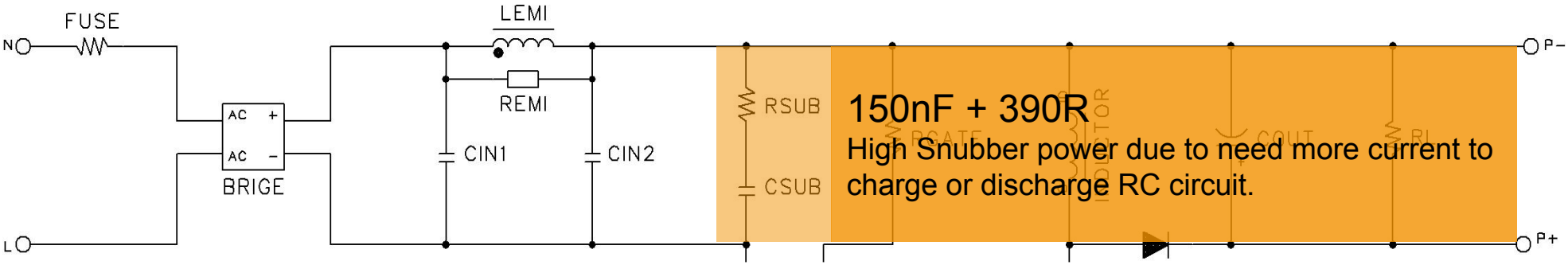


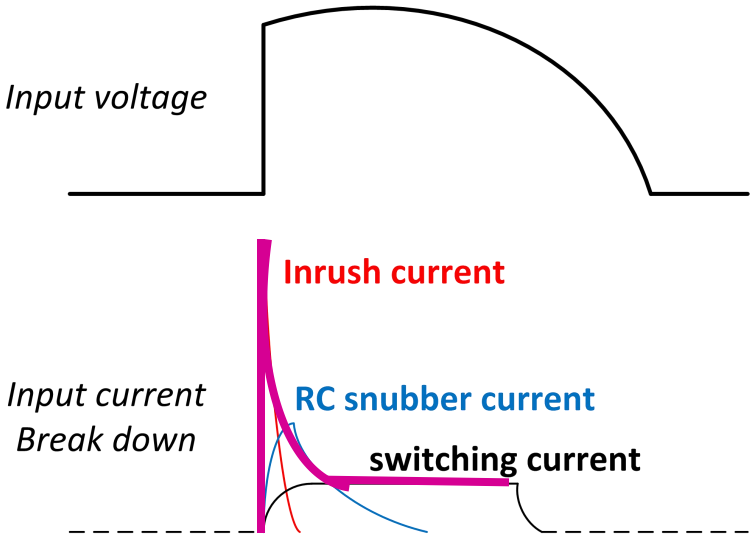
Rgate & Cgate Recommendation





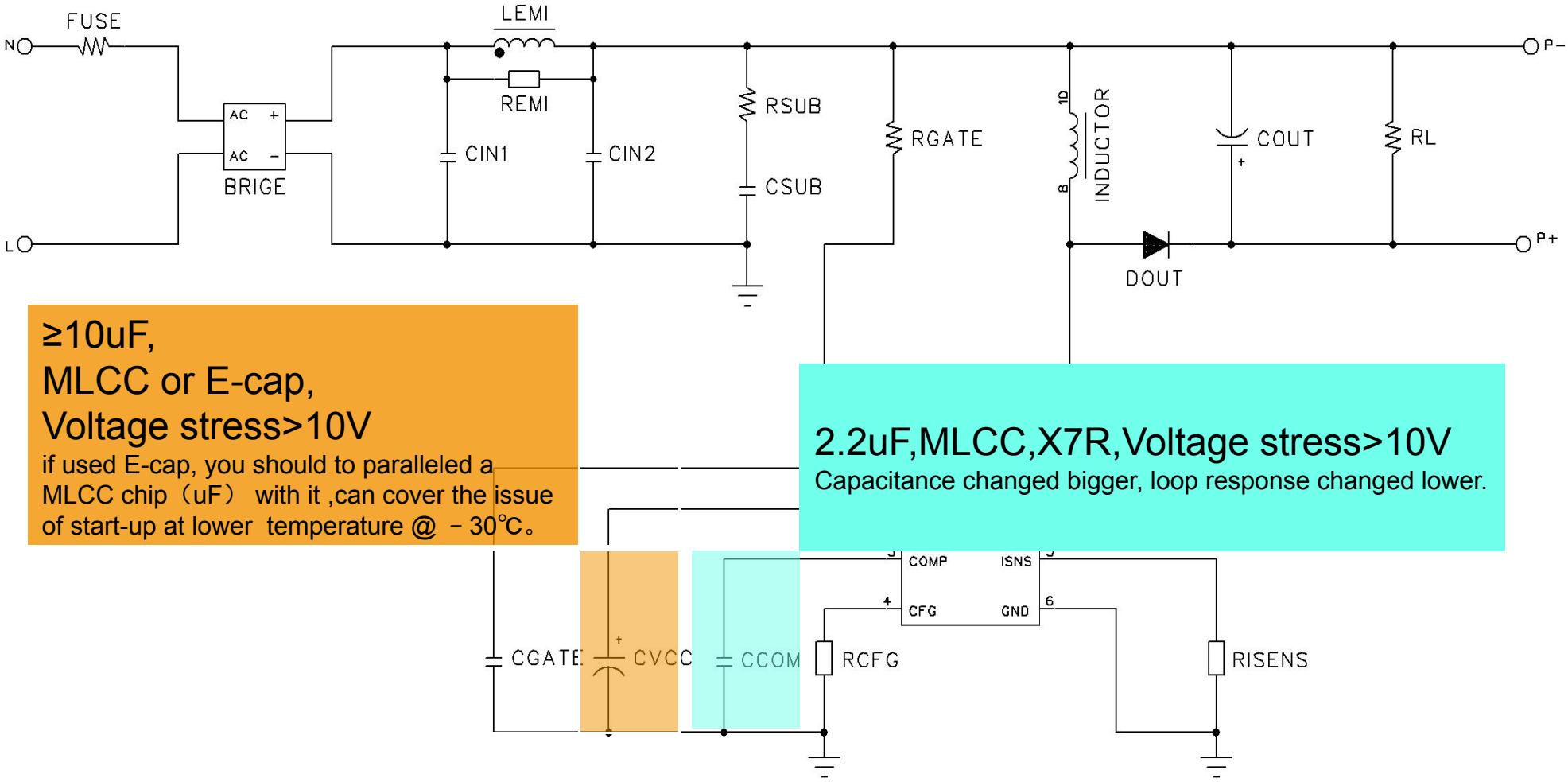
RC Recommendation





The peak of the inrush current spike is determined by the resistance and input voltage.
RC snubber circuit is to provide additional inrush current for latching the TRIAC in leading edge dimmer operation.
RC snubber circuit is designed to have a longer (about 10x) RC time constant but with lower peak current.

C_{VCC} & C_{COM} Recommendation



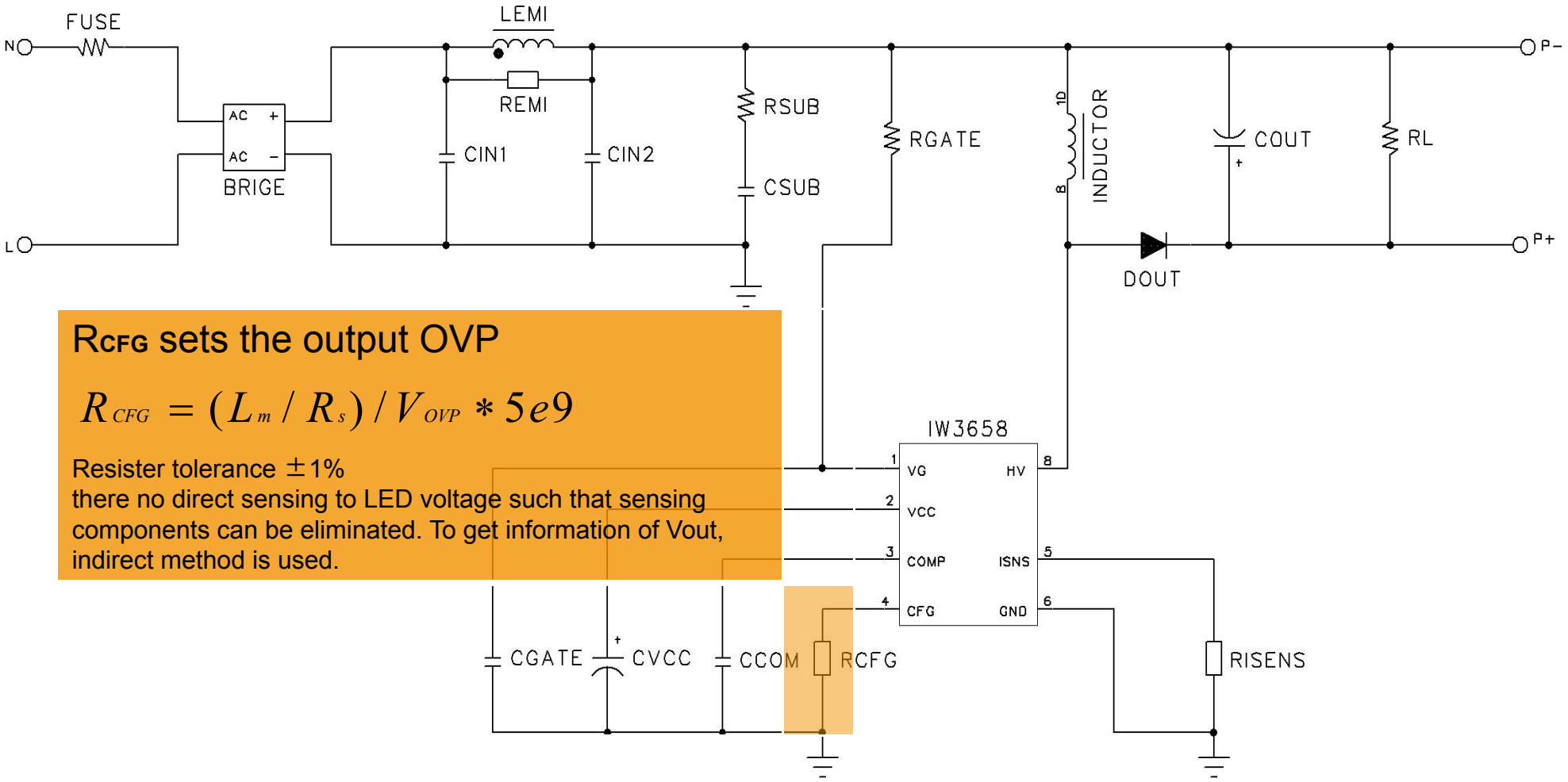
≥10uF,
MLCC or E-cap,
Voltage stress>10V

if used E-cap, you should to paralleled a MLCC chip（uF） with it ,can cover the issue of start-up at lower temperature @ －30℃。

2.2uF,MLCC,X7R,Voltage stress>10V

Capacitance changed bigger, loop response changed lower.

R_{CFG} Introduction



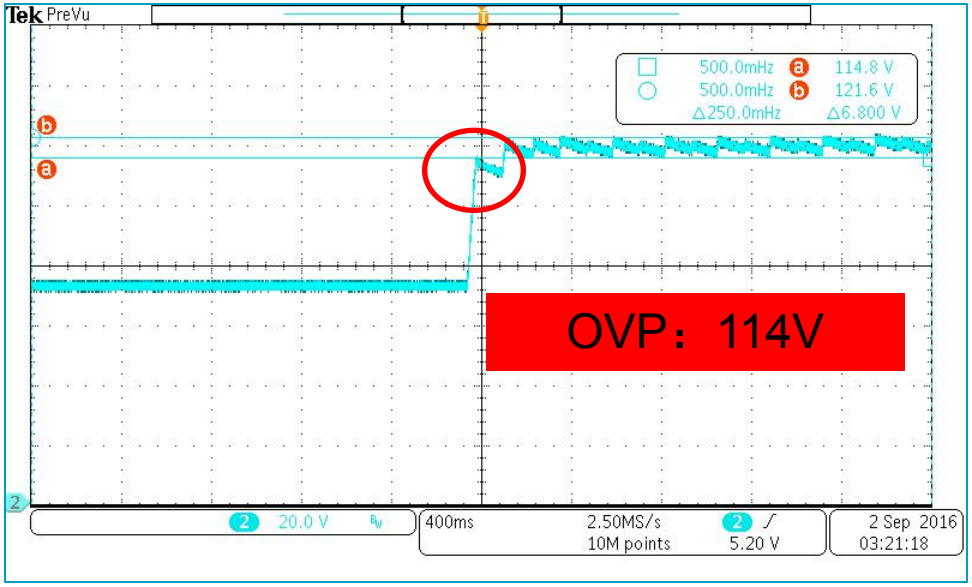
R_{CFG} sets the output OVP

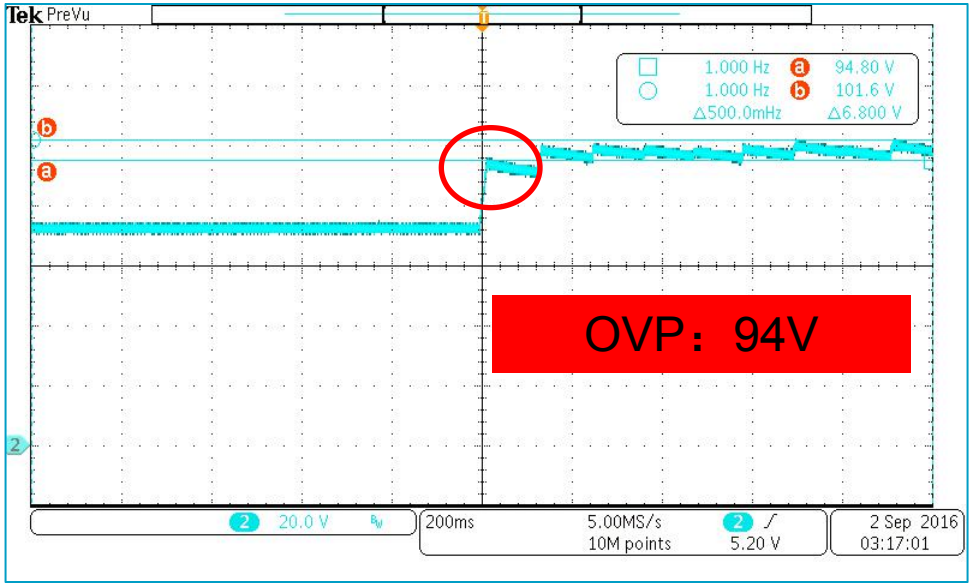
$$R_{CFG} = (L_m / R_s) / V_{OVP} * 5e9$$

Resister tolerance ±1%
there no direct sensing to LED voltage such that sensing components can be eliminated. To get information of Vout, indirect method is used.

As a sample of 72V120mA design, according calculate sheet,
CFG resister value range is 45.25KΩ-59.17KΩ,test OVP at these two condition.

CFG=47K	CFG=56K





So, CFG resister value will impact the OVP point, CFG value ↑， OVP point ↓。

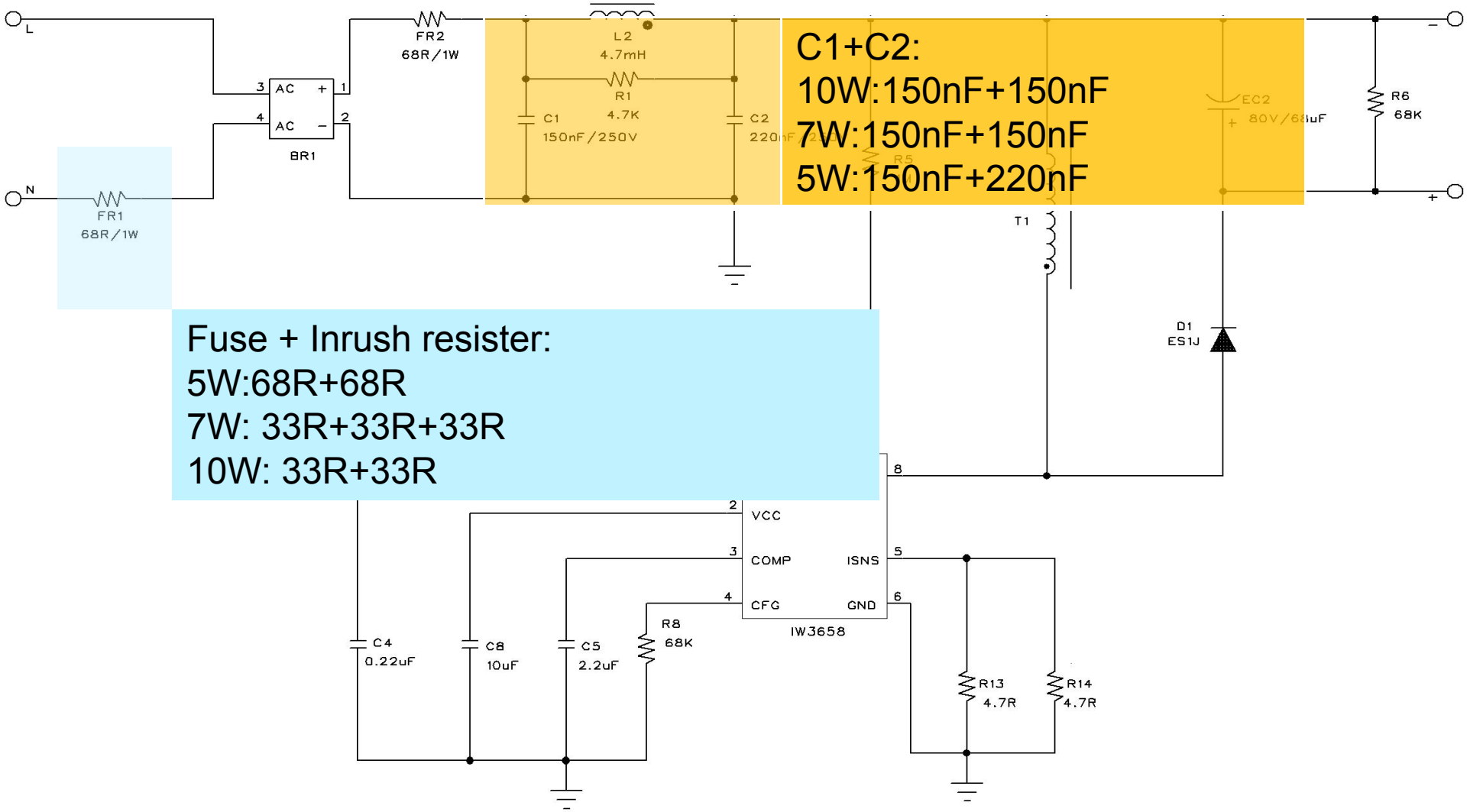
※ with some issue about OVP for AA sample. The point that marked by red is triggered OVP

In fact, when output voltage defined, OVP range had defined, Vipk-clamp voltage also be defined. Relationship of three parameters as below:

V_{IPK_CLAMP}		0.96 V	0.80 V	0.66 V
R_{CFG}		45.25KΩ - 59.17KΩ	59.17KΩ - 85.47KΩ	85.47KΩ - 128.2KΩ
NVo	Lm/Rs=1000u (buck-boost)	65 V - 80 V	45 V - 65 V	30 V - 45 V
	Lm/Rs=700u (buck)	46 V - 56 V	46 V - 32 V	21 V - 32 V

No RC damping

For low line and Power over 5W.



Sample test result with RC and without RC damping (57V75mA)

（No RC sample C1+C2=220nF+220nF, Fuse + Inrush=136Ω）

Input voltage (V)	Input Power (W)		PF		Iout (mA)		Vout (V)		Output Power (W)		Efficiency (%)	
	WITH	NO	WITH	NO	WITH	NO	WITH	NO	WITH	NO	WITH	NO
90	4.35	4.46	0.949	0.945	63.92	64.2	55.4	58	3.54	3.72	83.49	81.41
95	4.52	4.61	0.938	0.935	66.41	66.55	55.6	58.1	3.69	3.87	83.87	81.69
100	4.67	4.75	0.928	0.925	68.76	68.71	55.8	58.2	3.84	4	84.19	82.16
105	4.81	4.89	0.918	0.915	70.97	70.76	56	58.3	3.97	4.13	84.36	82.63
110	4.94	4.89	0.908	0.902	73.03	71.12	56.1	58.3	4.1	4.15	84.79	82.93
115	4.98	4.88	0.894	0.887	73.94	71.25	56.2	58.3	4.16	4.15	85.12	83.45
120	4.97	4.87	0.879	0.874	74.04	71.4	56.2	58.2	4.16	4.16	85.33	83.72
125	4.95	4.87	0.864	0.861	74.18	71.53	56.2	58.2	4.17	4.16	85.48	84.22
132	4.93	4.87	0.844	0.843	74.33	71.75	56.2	58.2	4.18	4.18	85.75	84.73

Efficiency changed lower 1~2%.

Dimming performance(57V75mA)

Without RC damping											
1	LEVITON	TRIMATRON	6681	LE	74.34	99.79%	6.5	8.72%	28	37.54%	
2	LUTRON	SKYLARK	CT-600	LE	65.75	88.26%	3.7	4.97%	3.7	4.96%	
3	LEVITON	SureSlide	6633	LE	74.32	99.76%	2.6	3.49%	2.6	3.49%	shimmer at minimum location
4	LUTRON	LUMEA	LG-600	LE	66.6	89.40%	2.9	3.89%	2.9	3.89%	
5	LUTRON	SKYLARK	S-600	LE	67	89.93%	1.2	1.61%	3	4.02%	
6	LEVITON	TRIMATRON	6683	LE	74.33	99.77%	0	0.00%	24	32.18%	shimmer at minimum location
7	LEVITON	SureSlide	6631	LE	70.4	94.50%	1	1.34%	7	9.39%	shimmer at minimum location
8	LUTRON	GLYDER	GL-600	LE	72.3	97.05%	3.6	4.83%	3.6	4.83%	
9	LEVITON	TRIMATRON	6602	LE	74.32	99.76%	0	0.00%	23.2	31.11%	shimmer at minimum location
With RC damping											
1	LEVITON	TRIMATRON	6681	LE	75.45	100.00%	5.38	7.13%	35	46.39%	
2	LUTRON	SKYLARK	CT-600	LE	67.4	89.33%	4.2	5.57%	4.2	5.57%	
3	LEVITON	SureSlide	6633	LE	75.35	99.87%	3	3.98%	3	3.98%	
4	LUTRON	LUMEA	LG-600	LE	68.1	90.26%	3.56	4.72%	3.56	4.72%	
5	LUTRON	SKYLARK	S-600	LE	68.34	90.58%	1.42	1.88%	9	11.93%	
6	LEVITON	TRIMATRON	6683	LE	75.4	99.93%	0	0.00%	29	38.44%	shimmer at minimum location
7	LEVITON	SureSlide	6631	LE	71.88	95.27%	1.1	1.46%	14	18.56%	shimmer at minimum location
8	LUTRON	GLYDER	GL-600	LE	73.85	97.88%	3.94	5.22%	9	11.93%	
9	LEVITON	TRIMATRON	6602	LE	75.4	99.93%	0	0.00%	28	37.11%	shimmer at minimum location

Dimming performance changed worse.

Key Feature

Typical Application Schematic

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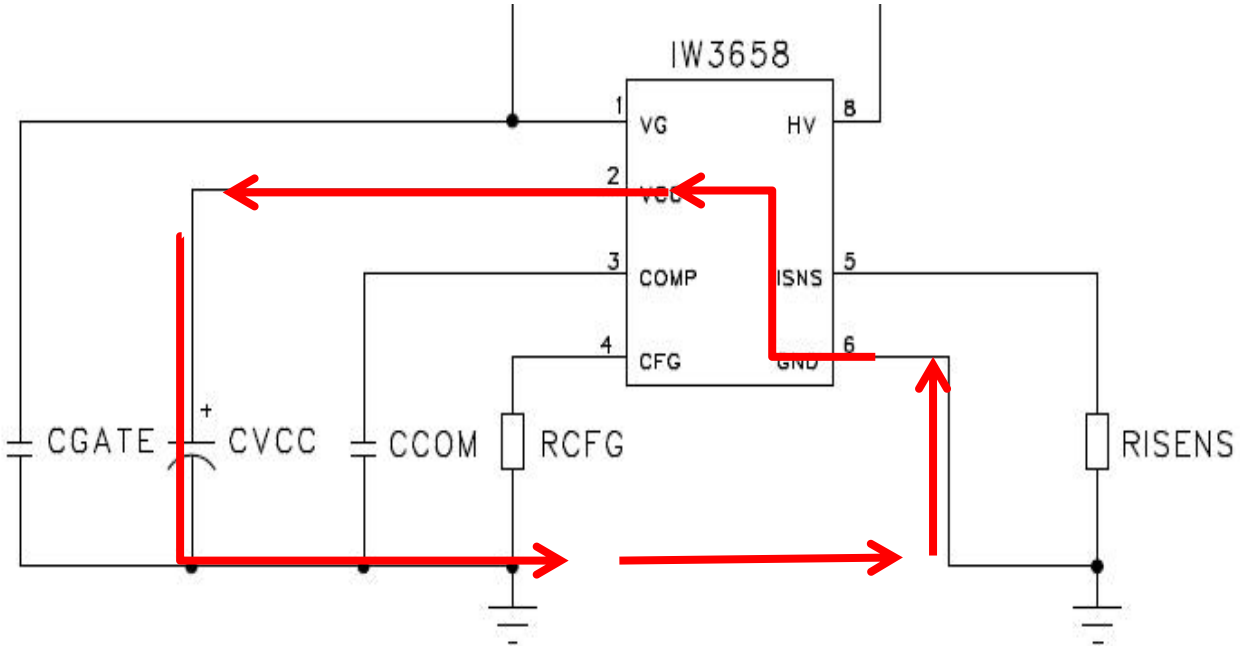
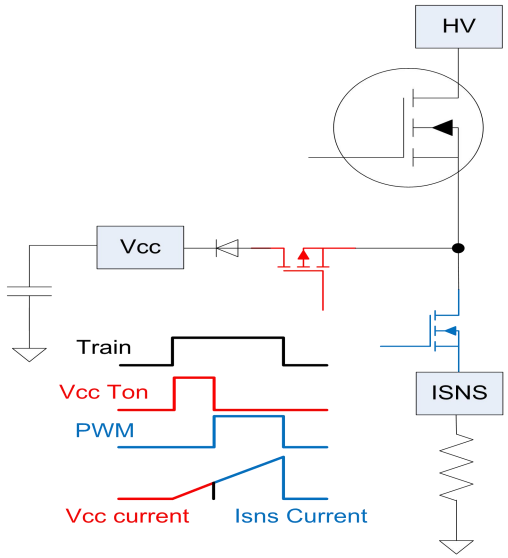
Summary

Vcc loop

In Sunstone, source-switching charging Vcc is used to supply Icc.
The Ton charge circuit is same as iW3688 and IW3689.



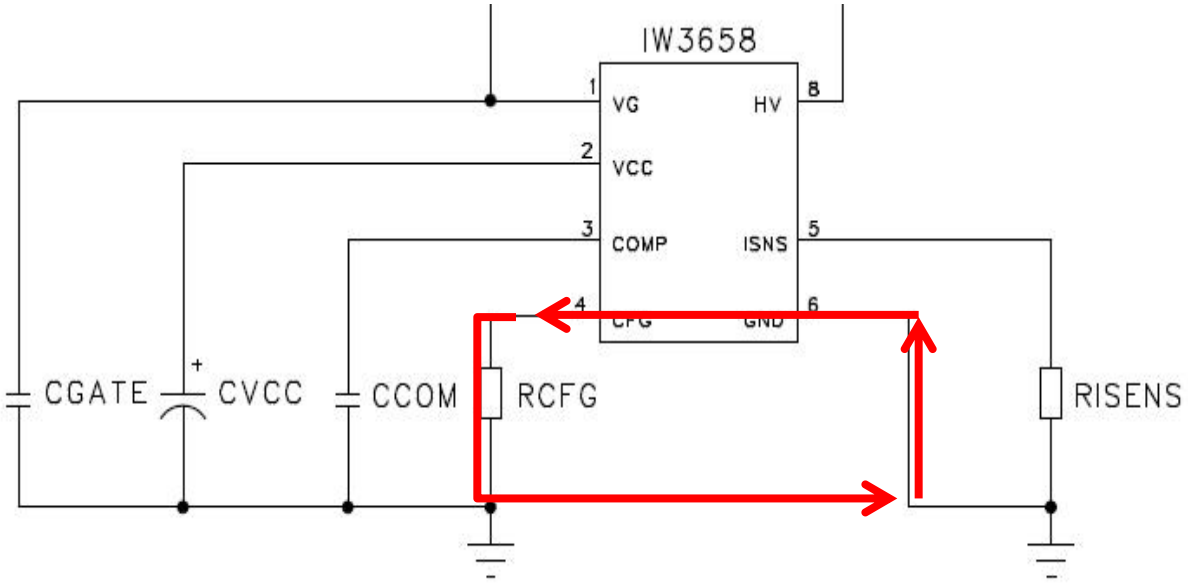
Vcc charge diagram



- ✓ Minimize the V_{CC} cap to IC GND pin trace.
- ✓ Minimize the V_{CC} cap to IC V_{CC} pin trace.

CFG Loop

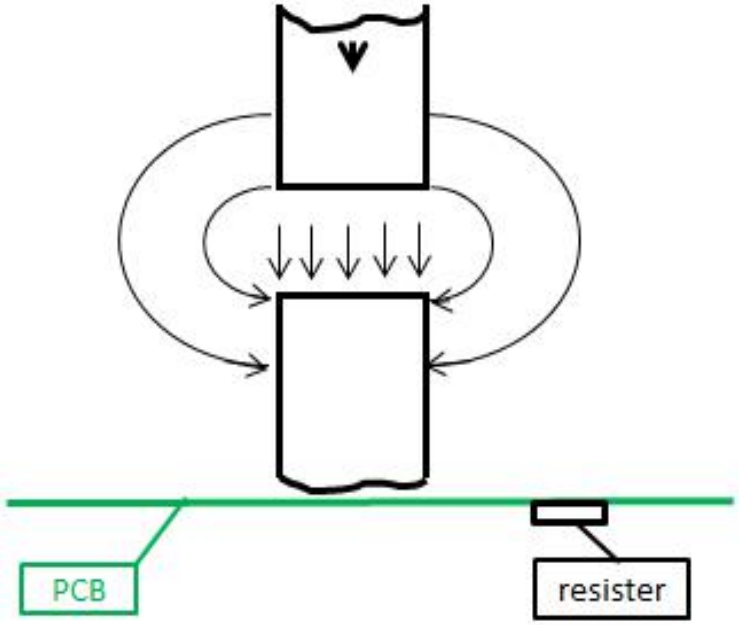
In Sunstone, there no direct sensing to LED voltage such that sensing components can be eliminated. To get information of Vout, indirect method is used.



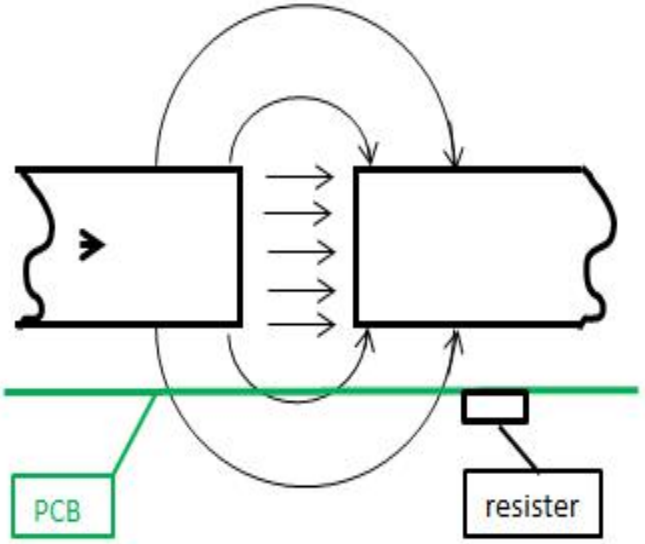
- ✓ Minimize the CFG resister to IC GND pin trace.
- ✓ Minimize the CFG resister to IC CFG pin trace.
- ✓ Keep far away CFG resister from transformer.
- ✓ Used Vertical transformer better than horizontal.

Electromagnetic interference impacted CFG sampling

Vertical transformer



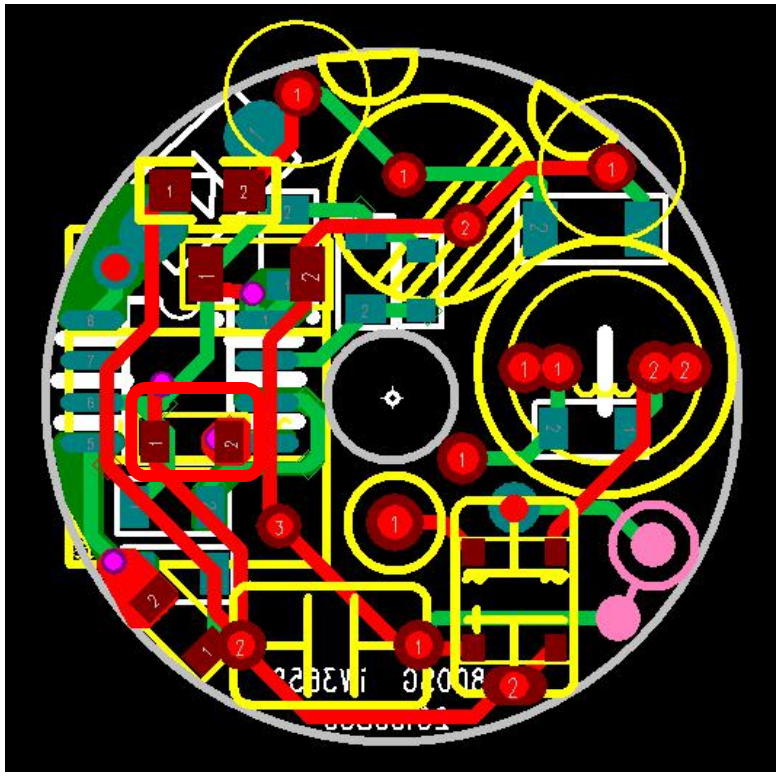
Horizontal transformer



※ the current across CFG resister with only a few uA.

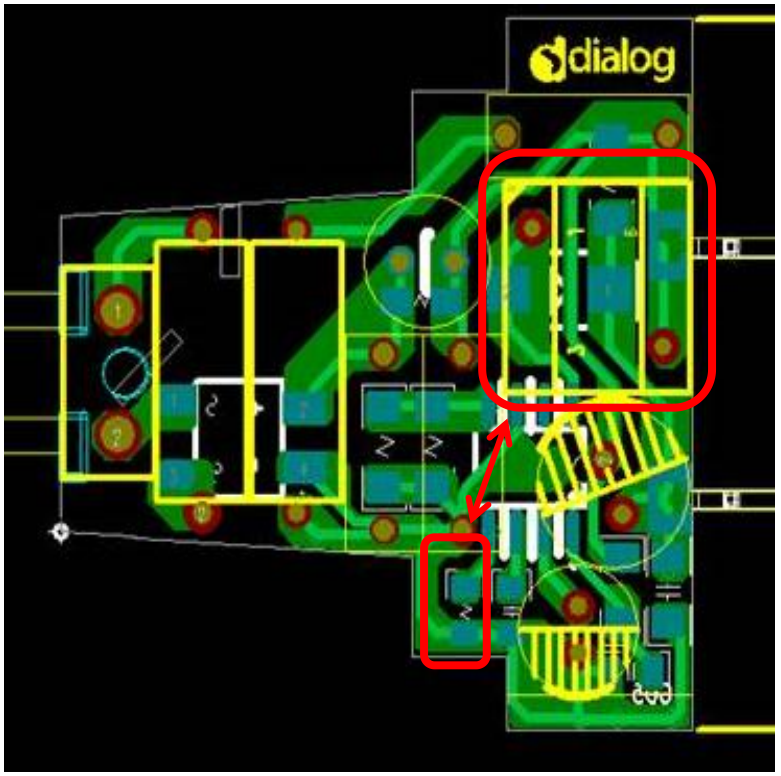
PCB layout for CFG loop

Bad layout



CFG resister at bottom of transformer with hole

Good layout



CFG resister far away from transformer

Key Feature

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Summary

OVP

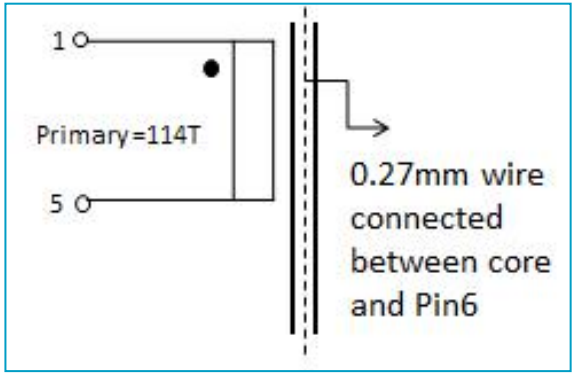
OVP out of control had mentioned, due to CFG Pin is very sensitive, easy to be interrupted by Layout and electromagnetic.

Solution :

✓ PCB layout

* Minimize the CFG resister to IC GND pin trace.
* Minimize the CFG resister to IC CFG pin trace.
* Keep far away CFG resister from transformer.
* Used Vertical transformer better than horizontal.

✓ Add shielding for transformer, connected it to Ground



Line regulation

At the dimmer condition, customer feedback output current cannot achieve 90% output current.

N0.	Make	Serial Number	Type	Max Iout(mA)	Max Iout Percentage	Min Iout(mA)	Min Iout Percentage
1	LUTRON	ANLV-600P	LE	109.81	**87.85%**	0.34	0.27%
2	LUTRON	LGCL-153PL	LE	109.35	**87.48%**	0.34	0.27%
3	COOPER	AIM06	LE	112.44	**89.95%**	7.11	5.69%
4	LUTRON	MACL-153M	LE	102.74	**82.19%**	12.16	9.73%
5	COOPER	T1306		97.15	**77.72%**	15.66	12.53%
6	LUTRON	CT-600	LE	110.39	88.31%	6.04	4.83%
7	LEVITON	SCL-153	LE	109.14	87.31%	6.90	5.52%
8	LUTRON	CTCL-153PD	LE	109.29	87.43%	30.96	24.77%
9	LUTRON	TGCL-153P	LE	111.59	89.27%	9.64	7.71%
10	LUTRON	NVLV-600P	LE	114.59	91.67%	16.91	13.53%
11	HUNTER	27182	TE	108.10	86.48%	12.11	9.69%
12	LUTRON	NTELV-300	TE	111.89	89.51%	19.00	15.20%
13	LEVITON	6842	LE	120.60	96.48%	0.00	0.00%

Solution:

✓ changed Lm lower, lead Ton higher

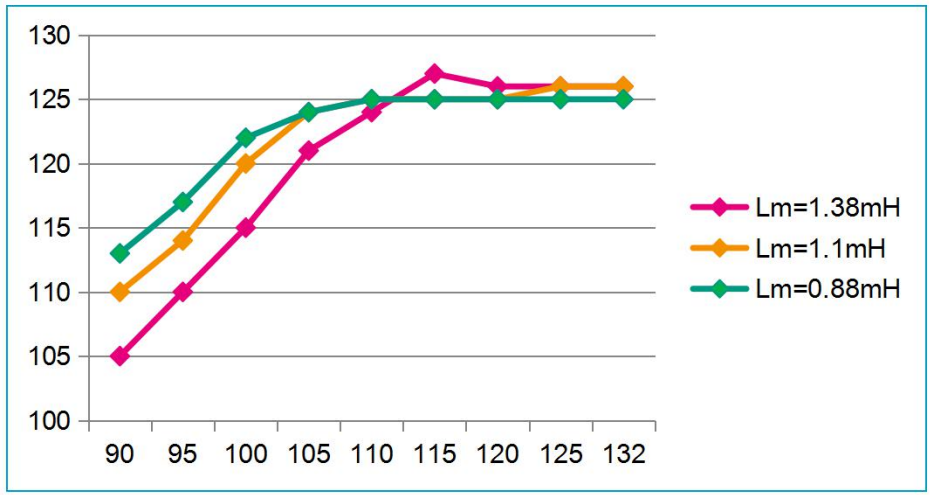
Line regulation

Adjust the value of (Lm/Rs) to test sample 72V125mA, test result as below:

Lm CFG	Input Voltage (Vac)	Input power (W)	PF	Iout (mA)	Vout (V)	Output power (W)	Efficiency (%)
CFG=50K Lm=1.38mH (Lm/Rs=1000)	90	9.48	0.9755	105	72	7.56	79.75
	95	9.88	0.9677	110	72	7.92	80.16
	100	10.26	0.9596	115	72	8.28	80.70
	105	10.67	0.9512	121	72	8.712	81.65
	110	10.97	0.9426	125	72	9	82.04
	115	11	0.9304	126	72	9.072	82.47
	120	10.94	0.9161	126	72	9.072	82.93
	125	10.88	0.9025	126	72	9.072	83.38
	132	10.82	0.8829	126	72	9.072	83.84
CFG=43K Lm=1.1mH (Lm/Rs=800)	90	10.02	0.9602	110	72	7.92	79.04
	95	10.4	0.9513	115	72	8.28	79.62
	100	10.74	0.9424	120	72	8.64	80.45
	105	11.04	0.9333	124	72	8.928	80.87
	110	11.12	0.9214	125	72	9	80.94
	115	11.04	0.9075	125	72	9	81.52
	120	10.98	0.894	125	72	9	81.97
	125	10.93	0.8807	126	72	9.072	83.00
	132	10.88	0.8632	126	72	9.072	83.38
CFG=30K Lm=0.88mH (Lm/Rs=600)	90	10.62	0.9366	113	72	8.136	76.61
	95	10.94	0.9267	117	72	8.424	77.00
	100	11.26	0.9171	122	72	8.784	78.01
	105	11.3	0.9045	124	72	8.928	79.01
	110	11.21	0.8907	125	72	9	80.29
	115	11.14	0.8777	125	72	9	80.79
	120	11.08	0.8651	125	72	9	81.23
	125	11.03	0.8527	125	72	9	81.60
	132	10.98	0.8365	125	72	9	81.97

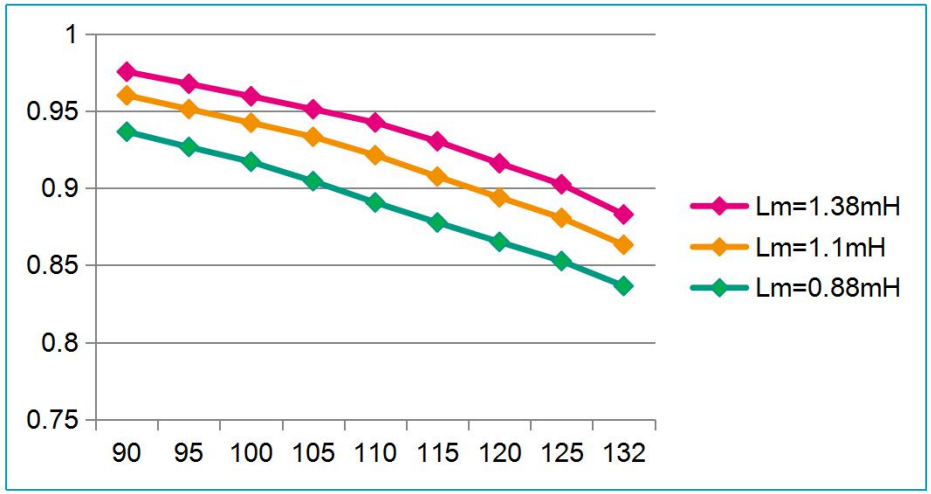
Line regulation

Line regulation Vs (Lm/Rs)

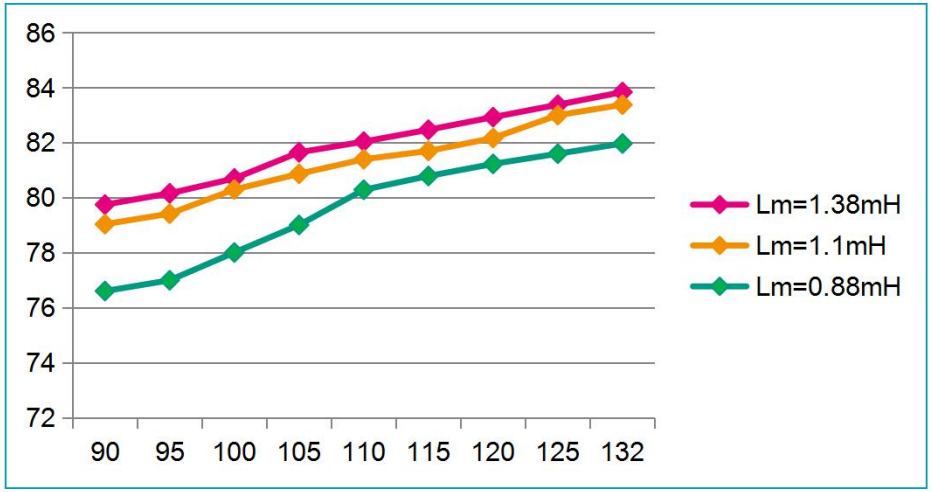


If you changed Lm lower,
Line regulation changed better;
Efficiency changed lower；
PF changed worse.

PF Vs (Lm/Rs)



Efficiency Vs (Lm/Rs)

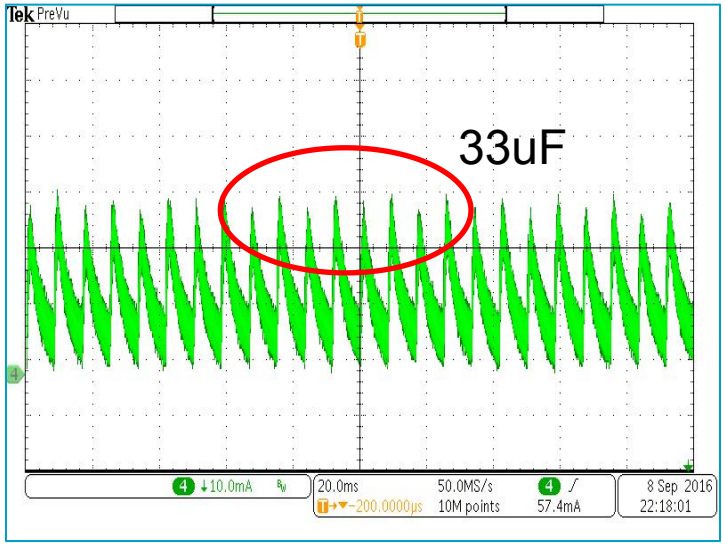


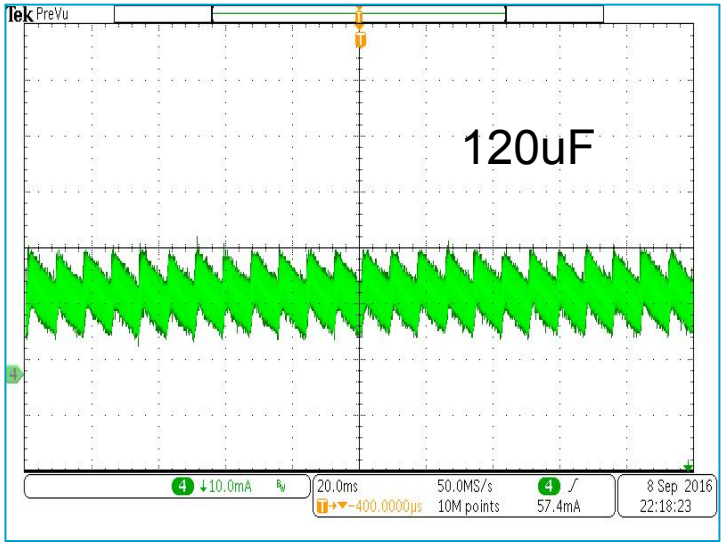
Shimmer

Most of dimmer is asymmetric at the minimum location, different from IW3689 and IW3688 can worked through automatic compensation of phase cut, Sunstone without this function at full process.

Solution：

✓ Add capacitance of output capacitor.

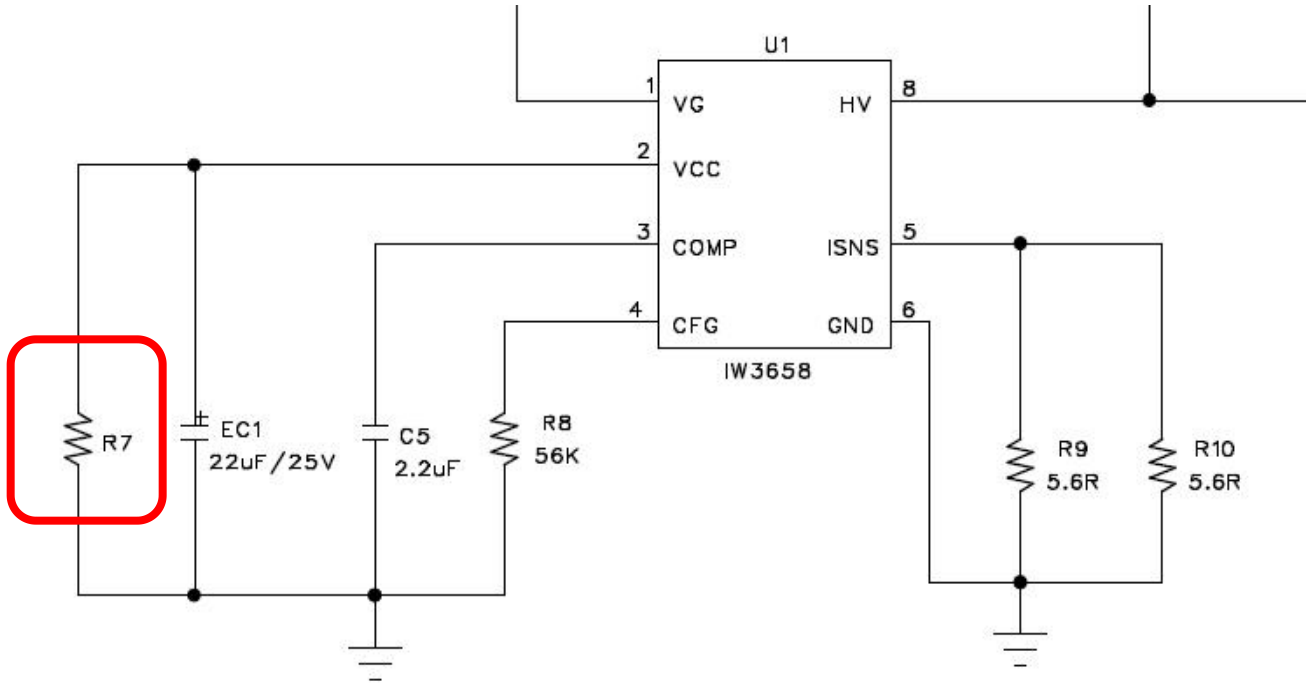




※Test sample at the same location of dimmer, only changed capacitance of output capacitor.

Shimmer

✓ Add bypass resister for Vcc capacitor

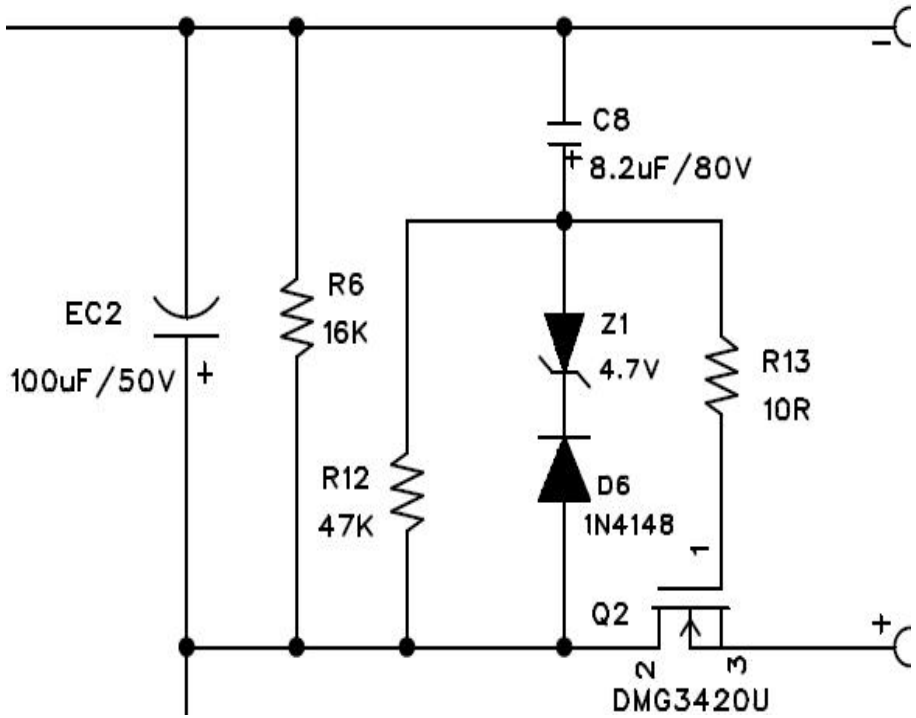


Add bypass resister for Vcc capacitor, to discharge at the minimum location to turn off the LED system. This solution will impact dimming range at minimum location.

Shimmer

✓ Add activity clamp circuit for output

Control MOS works in the constant current area.

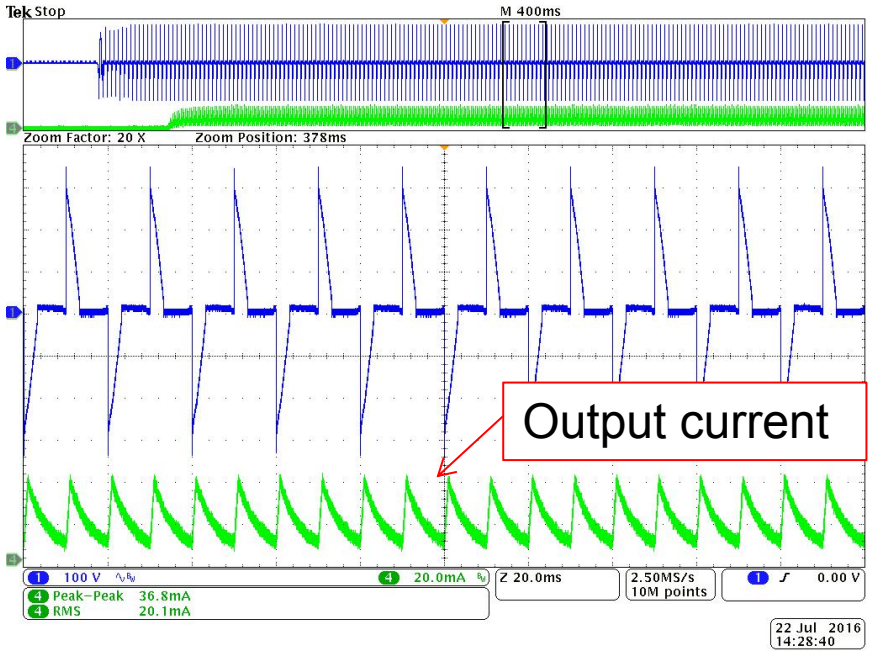


- C8 and R12 integral filter circuit, eliminating the power frequency voltage ripple
- D6 and Z1 play a role for fast charging C8, while D6 prevent C8 through the Z1 discharge, Z1 to prevent the C8 was over charging damage MOSFET
- R13 with the role to eliminate resonant

Shimmer

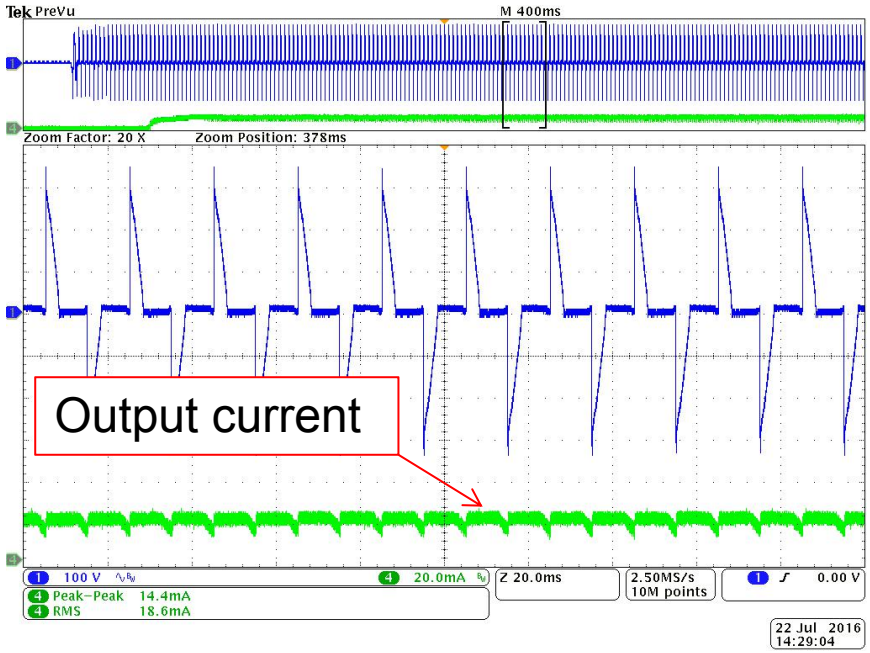
Compare clamp circuit with no clamp circuit

Without clamp circuit



Irip=36.8mA

With clamp circuit



Irip=14.4mA

DFMEA

DFMEA test result

Component		Fault Mode	Iin (mA)	Pin (W)	PF	Vo (V)	Io (mA)	Circuit Fault Effect	Effect to End-User
Vcc capacitor		short	3.3	0.21	0.52	0	0	no Vcc voltage	no output
		open	12.3	1.03	0.65	16.1	0	no Vcc voltage	no output
Compensation capacitor		short	10	0.7	0.55	0	0	lose Vipk reference voltage	no output
		open	62.7	7.3	0.97	68.6	94	no comp capacitor, Vipk turn low and less Iout	no effect
CFG resister		short	6	0.2	0.31	18.6	0	output voltage couldn't set up	no output
		open	18	0.69	0.32	59.3	6	OVP	shimmer
Isense resistor		short	0	0	0	0	0	FR1 opens, chip failure	no output
		open	11	0.3	0.2	50.9	0	OVP turn lower than output	no output
IW3658	Pin1 Isns	open	5.4	0.2	0.33	6	0	no switch loop	no output
	Pin1 Isns	short with pin2	72.9	0.3	0.34	0	0	FR1 opens, chip failure	no output
	Pin2 GND	open	0	0	0	0	0	FR1 opens, chip failure	no output
	Pin4 HV	open	0	0	0	0	0	no switch loop	no output
	Pin5 VG	open	0	0	0	0	0	no Vg voltage	no output
	Pin5 VG	short with pin6	0	0	0	0	0	Vg voltage cann't charge to MOS's Vth	no output
	Pin6 Vcc	open	3.3	0.2	0.52	0	0	no Vcc voltage	no output
	Pin6 Vcc	short with pin7	3.4	0.2	0.53	0	0	Vcc pull down by Comp to ULP	no output
	Pin7 comp	open	61	7.1	0.97	91	68.5	no comp capacitor, Vipk turn low and less Iout	no effect
	Pin7 comp	short with pin8	5.2	0.2	0.36	18	0	output voltage couldn't set up	no output
	Pin8 CFG	open	18	0.69	0.32	59.3	6	OVP	shimmer

Key Feature

Typical Application Schematic

Basic Application

Layout Consideration

Issue sharing

Calculate sheet introduction

Summary

Calculate Sheet introducetion

Step 1 : Choose input voltage 、 output voltage and current

客户应用设计规格						
详细名称	简称	单位	最小	典型	最大	备注
输入规格--高低压，地区	Region	N/A	北美，日本：100-120V			请选择应用范围
AC输入RMS电压	VAC	V	90	120	138	推荐浮动范围+-15%
AC输入频率	fAC	Hz	57	60	63	推荐浮动范围+-3Hz
LED电压范围	Vout	V	45	50	55	支持25V到80V之间
LED设计电流	Iout	A		0.12		
输出功率	Pout	W	5.40	6.00	6.60	PASS
输入功率	Pin	W	6.35	7.06	7.76	假定效率为85%
推荐使用的3658型号	PN	N/A		TBD		
推荐使用的拓扑结构	Topology	N/A	BUCK或BUCK-BOOST			230V推荐Buck-boost, 120V高输出电压用Buck-boost
选择使用的拓扑结构	Topology act	N/A	BUCK-BOOST			PASS
内部基准电压	Viref	V		0.35		
推荐电感量/Isns电阻比	Lm/Rs	u/ohm	800	1000	1200	
实际电感量/Isns电阻比	Lm/Rs	u/ohm		1000		

BUCK-BOOST或FLYBACK电感/变压器设计						
详细名称	简称	单位	最小	典型	最大	备注
电感/变压器原副边匝比	Ntr	N/A		1.00		3658使用简单电感
主电感量	Lm	uH	1316	1385	1455	需要控制在+-5%以内
电感/变压器的有效磁芯面积 (Ae)	**Ae**	**mm2**		**16.1**		**参照磁芯的说明书**
电感/变压器的最大磁通密度 (Bmax)	**Bmax**	**mT**		**340**		**参照磁芯的说明书，在100c下的最大磁通密度**
电感/变压器原边的匝数	Np	turn	121	175		PASS
电感/变压器副边的匝数	Ns	turn		175		
带调光器时Isns脚电压	Visns	V		0.630		
带调光器时电感原边峰值电流	**Ipk_dim**	**A**			**0.455**	
电感最大磁通量密度	Bmax_dim	mT			235	请确认电感不会饱和，如可能饱和，增加电感匝数

Input voltage
output voltage
output current

Choose buck or Buck-boost

Choose “1000”

Calculate Sheet introduction

Step 2 : Choose CFG resister

系统工作参数						
最长Ton时间	Ton(max)	uS			9	
最长Toff时间	Toff(max)	uS			400	当输出电压太低，IC无法检测到Valley时
AC顶点开关频率	Fsw	kHz	47	59		最低频率出现在调光时
输出开路OVP电压	**Vovp**	**V**	**59**	**68**	**76**	
输出短路功耗	**Pshort**	**W**		**0.483**		

非功率元件选择						
详细名称	简称	单位	最小	典型	最大	备注
Isense电阻	**Risns**	**ohm**		**1.39**		**使用1%电阻**
CFG电阻推荐值	**Rcfg**	**k ohm**	**66.7**	**74.1**	**81.5**	**使用1%电阻，会影响OVP精度**
实际CFG电阻	**Rcfg_act**	**k ohm**		**74**		**使用1%电阻，会影响OVP精度**
Gate上拉电阻	Rgate	k ohm		750		使用5%的电阻
Gate电容	Cgate	uF	0.15	0.22	0.33	使用X7R 0805电容
Comp电容	Ccomp	uF		2.2		使用X7R 0805电容
假负载电阻	**RL**	**k ohm**	**35.7**	**37.6**	**39.5**	**使用5%的电阻**

Vcc电容和Vcc负载						
详细名称	简称	单位	最小	典型	最大	备注
Vcc电容	CVcc	uF	22	22	33	使用电解电容，无须0.1uF瓷片电容，10V或以上
Vcc负载	RVcc	k ohm		TBD		避免buck-boost最底端微闪

功率元件的选择						
详细名称	简称	单位	最小	典型	最大	备注
输出二极管耐压	Vdiode	V		600		ES1J
电桥耐压	Vbridge	V	600		1000	MB6S

Choose the resister value in the range

Calculate Sheet introduce

Step 3 : transformer parameters defined

BUCK-BOOST或FLYBACK电感/变压器设计						
详细名称	简称	单位	最小	典型	最大	备注
电感/变压器原副边匝比	Ntr	N/A		1.00		3658使用简单电感
主电感量	Lm	uH	1316	1385	1455	需要控制在+-5%以内
电感/变压器的有效磁芯面积 (Ae)	**Ae**	**mm2**		**16.1**		**参照磁芯的说明书**
电感/变压器的最大磁通密度 (Bmax)	**Bmax**	**mT**		**340**		**参照磁芯的说明书，在100C下的最大磁通密度**
电感/变压器原边的匝数	Np	turn	142	175		PASS
电感/变压器副边的匝数	Ns	turn		175		
带调光器时Isns脚电压	Visns	V		0.740		
带调光器时电感原边峰值电流	**Ipk_dim**	**A**			**0.534**	
电感最大磁通量密度	Bmax_dim	mT			276	请确认电感不会饱和，如可能饱和，增加电感匝数

系统工作参数						
最长Ton时间	Ton(max)	uS			9	
最长Toff时间	Toff(max)	uS			400	当输出电压太低，IC无法检测到Valley时
AC顶点开关频率	Fsw	kHz	47	59		最低频率出现在调光时
输出开路OVP电压	**Vovp**	**V**	**59**	**68**	**76**	
输出短路功耗	**Pshort**	**W**		**0.483**		

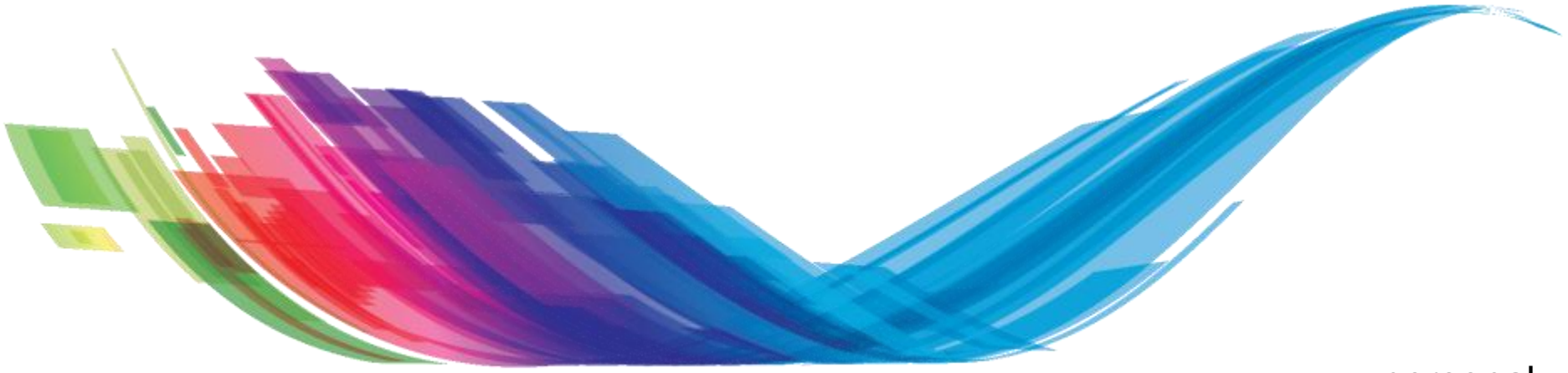
Turn number, inductance

Other parameters you can refer the sheet directly when you finished these 3 steps.

Summary

- ✓ Application is simply, easy to do design.
- ✓ CFG, Output voltage and Clamp voltage relationship can help to review your design.
- ✓ No RC damping application impacted efficiency and dimming performance.
- ✓ Pay more attention about PCB layout.

The Power To Be…



…personal
…portable
…connected